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**UNIVERSITY OF MORATUWA**

**FACULTY OF ENGINEERING**

**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**

B.Sc. Engineering

2015 Intake Semester 2 Examination

**CS2052 COMPUTER ARCHITECTURE**

Time allowed: 2 Hours

January 2017

**ADDITIONAL MATERIAL:** *None*

**INSTRUCTIONS TO CANDIDATES:**

1. This paper consists of **13** pages.
2. Answer **ALL** questions.
3. Answer the questions on the paper itself. **DO NOT** exceed the given space.
4. Applicable Assembly instructions are given as **Annex**.
5. For MCQ and True/False questions, select the most appropriate answer. No penalty for wrong answers.
6. The maximum attainable mark for each question is given in brackets.
7. This examination accounts for 50% of the module assessment.
8. This is a closed book examination.

***NB: It is an offence to be in possession of unauthorised material during the examination.***

9. Only calculators approved by the Faculty of Engineering are permitted.
10. Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions made on the script.
11. In case of any doubt as to the interpretation of the wording of a question, make suitable assumptions and clearly state them on the script.
12. This paper should be answered only in English.

Q1	Q2	Q3	Q4	Total

**Question 1**

**[25 marks]**

Figure 1 shows the block diagram of a simple microprocessor (a.k.a. nano-processor). Answer following questions based on Figure 1.

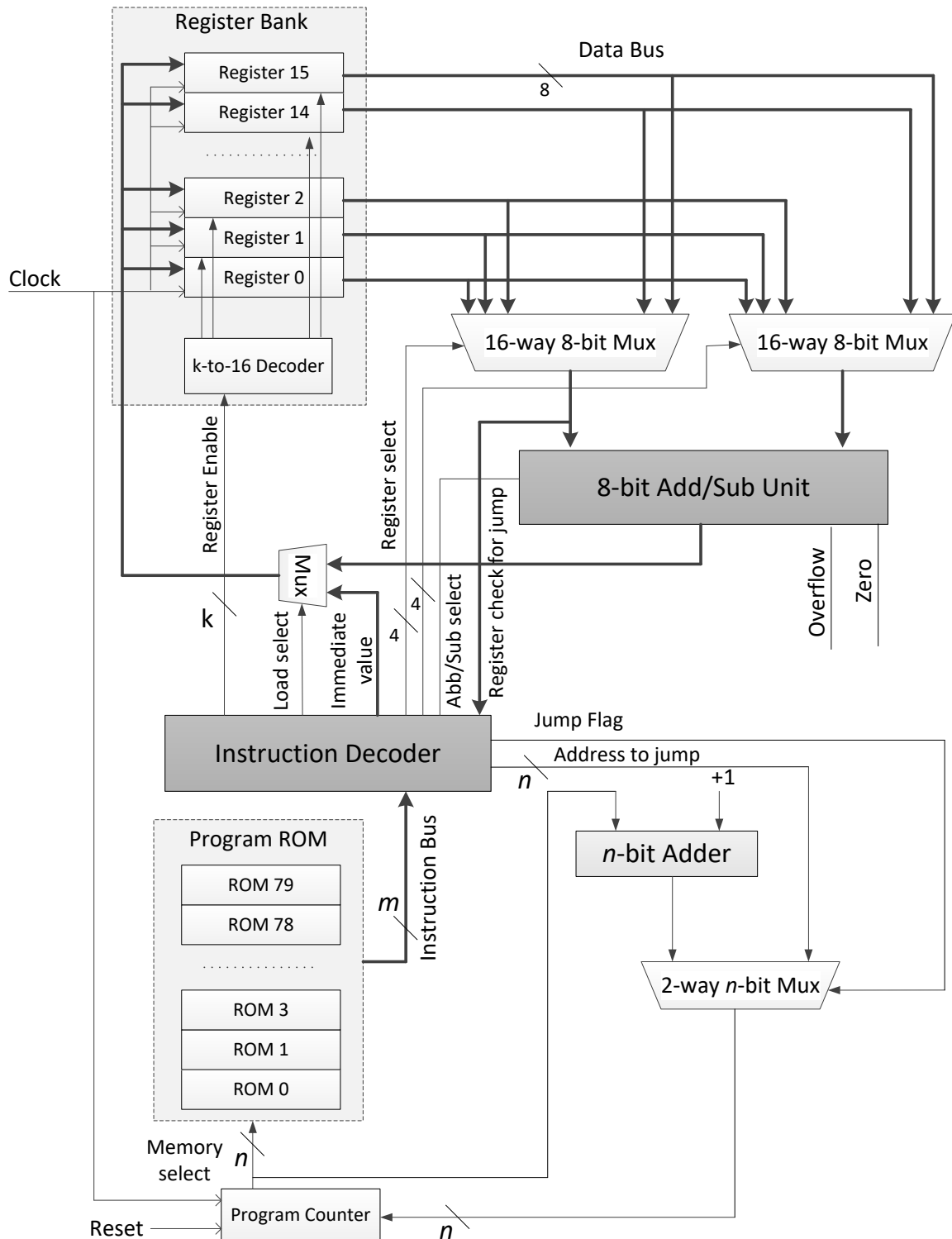


Figure 1 – High-level diagram of the microprocessor.

- (i) “This microprocessor design is based on the Harvard Architecture”. [1 mark]  
 True                      False



(viii) Once the instruction in (vi) above is decoded, what bit values will you set for each of the following as control inputs? [4 marks]

16-way 8-bit Mux connected to left input of Add/Sub Unit

16-way 8-bit Mux connected to right input of Add/Sub Unit

Register Enable

Abb/Sub Select

(ix) Once the instruction GOTO 50 is decoded, what bit values will you set for each of the following as control inputs? [2 marks]

Jump Flag  Address to Jump

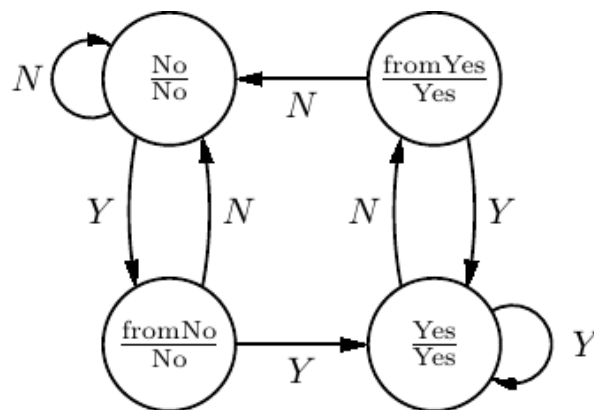
(x) Write an Assembly program to perform the following calculation using the instructions given in **Table 1**. You may use the general-purpose registers in Figure 1 to store intermediate and final results. Comment your code. [5 marks]

$-12_{10} - 19_{10}$

**Question 2**

[25 marks]

Consider the following state transition diagram of a 2-bit predictor.



A 2-bit predictor predicts whether a conditional branch (e.g., BTFSS) is likely to be taken or not, in the future. The predictor continues to predict the same outcome, taken or not taken the branch, until it makes 2 mistakes in a row. **Y** indicates when the branch is taken and **N** indicates when it is not. The notation in the state bubble has the format *state/output*. For example, *fromNo/No* means this state is reached from No state (*fromNo*) and output is *No*.

Let us label the states as 00 – No 01 – *fromNo* 10 – *fromYes* 11 – Yes

Let input **Y** be 1 and **N** be 0.

- (i) Fill in the following state transition table.

[4 marks]

Current State		Input		Next State	
	S <sub>1</sub>	S <sub>0</sub>	Y/N	S <sub>1</sub>	S <sub>0</sub>
<i>No</i>	0	0	0		
	0	0	1		
<i>fromNo</i>	0	1	0		
	0	1	1		
<i>fromYes</i>	1	0	0		
	1	0	1		
<i>Yes</i>	1	1	0		
	1	1	1		

- (ii) Let us build the 2-bit predictor using a set of JK flip-flops. Fill in the blanks of the following binary state table to obtain the desired output.

[5 marks]

Current State		Input	Next State			
S <sub>1</sub>	S <sub>0</sub>	Y/N	J <sub>1</sub>	K <sub>1</sub>	J <sub>0</sub>	K <sub>0</sub>
0	0	0	0	X	0	X
0	0	1	0	X		
0	1	0	0	X		
0	1	1			X	0
1	0	0				
1	0	1				
1	1	0				
1	1	1			X	0

- (iii) Use following Karnaugh maps to derive simplified equations for each of the JK flip-flop inputs. [6 marks]

<b>J<sub>0</sub></b>	<b>S<sub>1</sub>S<sub>0</sub></b>			
<b>Y/N</b>	00	01	11	10
0				
1				

<b>K<sub>0</sub></b>	<b>S<sub>1</sub>S<sub>0</sub></b>			
<b>Y/N</b>	00	01	11	10
0				
1				

<b>J<sub>1</sub></b>	<b>S<sub>1</sub>S<sub>0</sub></b>			
<b>Y/N</b>	00	01	11	10
0				
1				

<b>K<sub>1</sub></b>	<b>S<sub>1</sub>S<sub>0</sub></b>			
<b>Y/N</b>	00	01	11	10
0				
1				

- (iv) Draw the circuit to implement the 2-bit predictor. Clearly label the circuit. [4 marks]

- (v) Consider the following C-style code.

```
int i = 0;
int a[1000];
for (i = 0, i < 1000, i++)
    a[i] = 2*i;
```

Suppose above program is to be implemented using the PIC instruction set. How many clock cycles will be wasted due to branch penalty? Justify. [3 marks]

*Hint:* PIC instructions have a branch penalty of 1 clock cycle, (i.e., where the pipeline needs to be flushed when the branch jump to somewhere else in the code, other than the next instruction).

- (vi) Above 2-bit predictor is to be used to reduce the branch penalty of question (v) by remembering what happened in the last 2 iterations. How many clock cycles will be wasted if 2-bit predictor is used? Justify. [3 marks]

*Hint:* If it is predicted not taken (*No* state), PC value will be used as usual. If it is predicted taken (*Yes* state), destination address will be used from the instruction without a delay. Assume 2-bit predictor starts with *No* state.

### Question 3

[25 marks]

- (i) Represent 173.205 using Single Precision, IEEE Floating Point standard. [4 marks]

*Hint:* Single Precision standard has a 23-bit mantissa, 8-bit exponent, and 1-bit sign. The exponent is calculated as  $E = e + 127$ .

- (ii) In 2's complement, if sum of 2 negative numbers yields a positive result, sum has \_\_\_\_\_ . (fill in blank) [1 mark]
- (iii) \_\_\_\_\_ was designed to overcome limitation of number of characters in ASCII. (fill in blank) [1 mark]
- (iv) Which of the following statements is **not true** about cache memory? [2 marks]
1. Cache memory occupy more chip space, as it is built using static RAM.
  2. Only programs with spatial locality benefits from caching.
  3. Fully associative caches typically reduce average memory access time.
  4. Least frequently used cache replacement policy requires a set of counters.
- (v) For a given application, 30% of the instructions require memory access. Instruction miss rate is 1% and data miss rate is 4%. L1 cache access time is 2 clock cycles while RAM access time is 30 clock cycles. Cache block size is 4 words.
1. How much time is required to access a word that is not in cache? [2 marks]
    - a) 2 clock cycles
    - b) 30 clock cycles
    - c) 32 clock cycles
    - d) 122 clock cycles
  2. What is the average memory access time for instructions? [2 marks]
    - a) 2 clock cycles
    - b) 2.32 clock cycles
    - c) 3.22 clock cycles
    - d) 30 clock cycles
  3. What is the average memory access time for data? [2 marks]
    - a) 2 clock cycles
    - b) 3.304 clock cycles
    - c) 4 clock cycles
    - d) 5.284 clock cycles
- (vi) Given an integer  $x$ , write an Assembly program to identify whether  $x$  is even (logical 1) or odd (logical 0). For example, if  $x = 3$ , a designated register should contain 0. Assume microprocessor has 20, 8-bit general purpose registers labelled as R1, R2, ... R20.  $x \in [0, 127]$ . It is ok to assume  $x$  is already stored in a general-purpose register. Use only the instruction set given as **Annex**. Comment your code. [7 marks]



- (vii) Following program multiply add matrices  $a$  and  $b$ , and store the result in  $c$ . How would you improve the program while benefiting from spatial and/or temporal locality in caching? Discuss while presenting an optimized program. [4 marks]

```
for (i= 0; i < m; i++)
  for (j = 0; j < n; j++)
    c[j][i] = a[j][i] * b[j][i]
```

#### Question 4

[25 marks]

Answer the questions in the context of following article.

AMD's new Zen CPU architecture is to be launched in early 2017. The first Zen chips, named as "Summit Ridge", will be produced on a 14nm FinFET process, with an 8-core/16-thread CPU. On recent testing, it outperformed 8Core/16Thread Intel Core i7-6900K CPU at the same clock speed.

Architecture-wise Zen is a brand new design. Clustered multithreading (CMT) used by AMD earlier is out; simultaneous multithreading (SMT), which has been used to great effect by Intel, is in. Zen will have a "new cache memory hierarchy with 8MB of L3 cache" with an enhanced pre-fetcher, a large unified L2 cache, and separate low-latency L1 instruction and data caches. AMD have doubled the bandwidth available to its L1 and L2 cache, while improving L3 cache bandwidth by 5× times what was available on its previous cache design.

The combination of better core engine and better cache system allow getting 40% IPC (Instructions Per Cycle) uplift. Zen uses an Artificial Intelligence to predict what future pathway an application will take (i.e., execution path) based on past executions. Smart Prefetch is a learning algorithm that tracks software behaviour to anticipate the data needs of an application and prepare the data into cache in advance.

Thermal Design Power (TDP) of Zen is 95W, whereas Intel equivalent uses 140W. Zen uses aggressive clock gating with multi-level regions to make sure sub-circuits are switches off when they are not in use. Zen has a feature called Extended Frequency Range (XFR), which looks to be a Turbo Speed like feature in Intel chips that scales along with the thermal headroom available to the CPU. Such precise

performance/power control is achieved using more than 100 embedded sensors with high accuracy, which enable optimal voltage, clock frequency, and operating mode with minimal energy consumption.

– Parts of the write up are extracted from [www.pcgamesn.com](http://www.pcgamesn.com) and [www.v3.co.uk](http://www.v3.co.uk)

- (i) AMD’s Zen is based on the Superscalar Architecture. [1 mark]  
True            False
- (ii) One way to double the bandwidth available to L1 and L2 cache is to use a memory bus that is  $2\times$  wide. [1 mark]  
True            False
- (iii) One way to increase L3 bandwidth is to increase the clock speed of the memory bus by  $5\times$  times. [1 mark]  
True            False
- (iv) Zen’s performance is  $1.1\times$  higher compared to Intel Core i7 with the same clock speed. How efficient is Zen compared to Intel i7 in terms of performance-to-power gain? [2 marks]
- |                 |                 |
|-----------------|-----------------|
| a) $0.71\times$ | b) $1.1\times$  |
| c) $1.16\times$ | d) $1.62\times$ |
- (v) Which of the following statements are correct? [2 marks]
1. Reducing voltage and clock rate reduce power
  2. Static power is reduced by switching off components that are not in use
  3. Extended Frequency Range (XFR) allow Zen to run on high-frequency for a short time
- |                 |                 |
|-----------------|-----------------|
| a) 1 and 2 only | b) 1 and 3 only |
| c) 2 and 3 only | d) 1, 2, and 3  |
- (vi) With the suggested changes, overall speed up of memory sub-system is estimated to be  $2.4\times$ . If waiting time for memory is 60% of the total time, what is the speed up of the overall system? [2 marks]
- Hint: You may use the Amdahl’s law to calculate the speed up.*

$$Speedup_{Overall} = \frac{1}{(1 - Fraction_{Enhanced}) + \frac{Fraction_{Enhanced}}{Speedup_{Enhanced}}}$$

- |         |         |
|---------|---------|
| a) 0.65 | b) 1.54 |
| c) 1.67 | d) 2.4  |

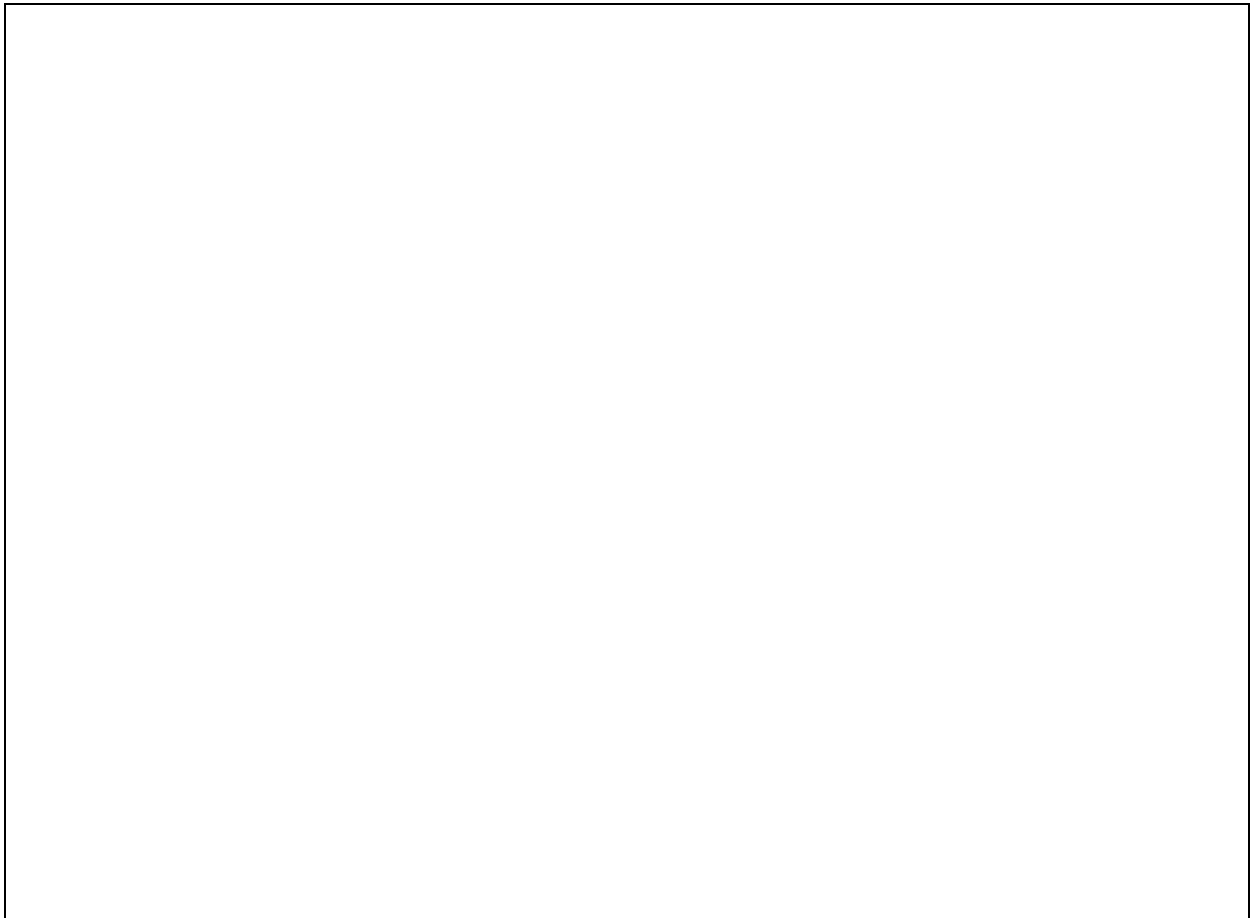
(vii) For what type of systems and applications will Zen be more suitable? Justify. [3 marks]

*Hint:* Consider options such as mobile devices, laptops, desktops, servers, and super computers.

(viii) Briefly describe the difference between threads and cores of a CPU. [3 marks]

(ix) Using an example explain what prefetching is? [3 marks]

- (x) Draw the cache hierarchy of Zen CPUs. Clearly label the diagram. [4 marks]



- (xi) *“While AMD has not announced about the number of stages in the Zen pipeline, we believed that it reduced from the previous generation of AMD chips”.*

Do you agree or disagree with this statement? Briefly discuss. [3 marks]



----- END OF THE PAPER -----