Index No:							

UNIVERSITY OF MORATUWA

Faculty of Engineering

Department of Computer Science & Engineering

B.Sc. Engineering
2016 Intake Semester 2 Examination

CS2052 COMPUTER ARCHITECTURE

Time allowed: 2 Hours December 2017

ADDITIONAL MATERIAL: *None*

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **4** questions on **12** pages.
2. This examination accounts for 60% of the module assessment.
3. This is a closed book examination.
4. Answer **ALL** questions.
5. Answer the questions on the paper itself. **DO NOT** exceed the given space.
6. Applicable Assembly instructions are given as **Annex**.
7. For MCQ and True/False questions, select the most appropriate answer. No penalty for wrong answers.
8. The maximum attainable mark for each question is given in brackets.
9. Only calculators approved by the Faculty of Engineering are permitted.
10. Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions made on the script.
11. If you have any doubt as to the interpretation of the wording of a question, make your own decision, but clearly state it on the script.
12. Electronic/Communication devices are not permitted. Only equipment allowed is a calculator approved and labelled by the Faculty of Engineering.
13. This paper should be answered only in English.

Q1	Q2	Q3	Q4	Total

Question 1 **[25 marks]**

Figure 1 shows the block diagram of a simple microprocessor (a.k.a. nano-processor). Answer following questions based on Figure 1.

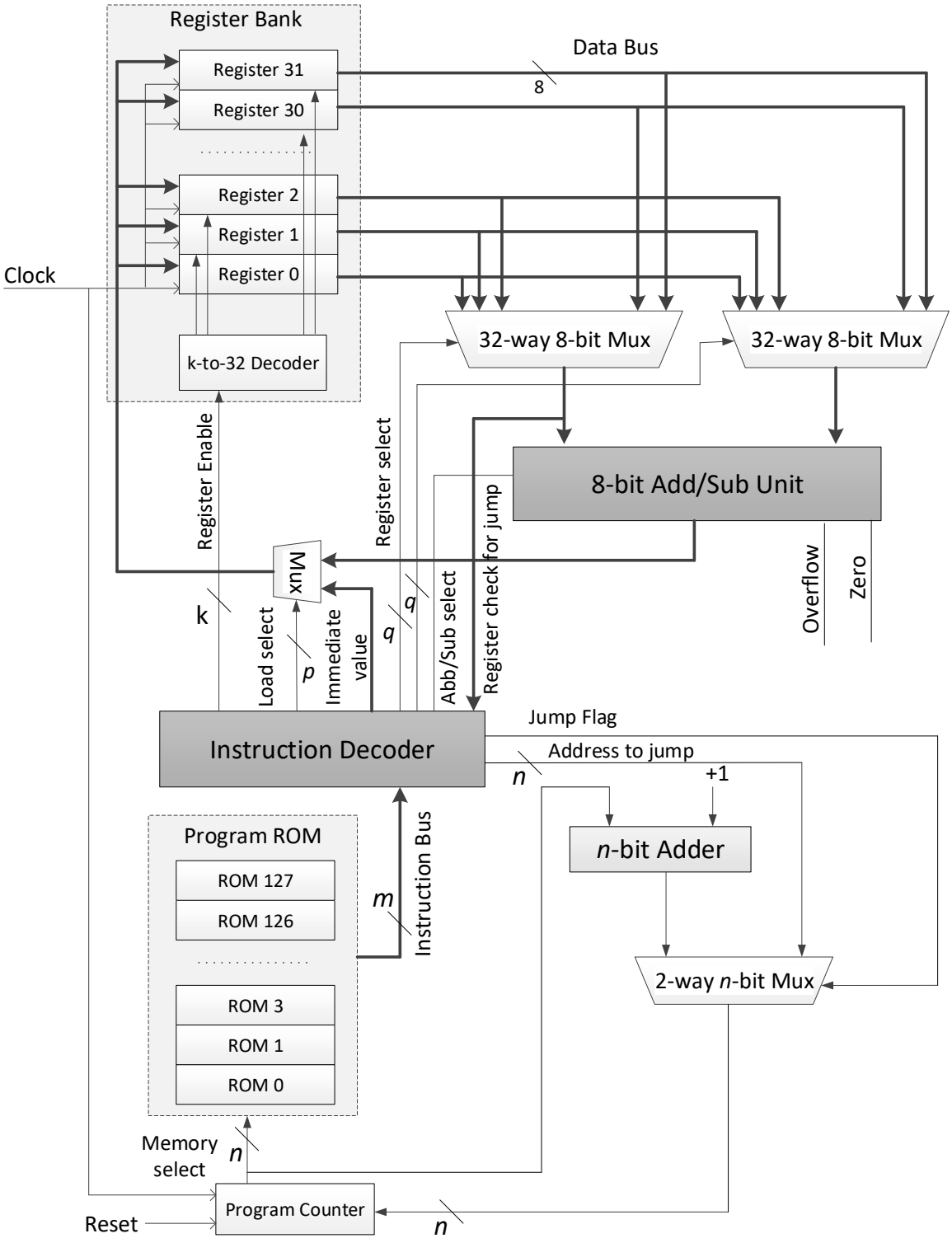

Figure 1 – High-level diagram of the microprocessor.

(i) Each 32-way 8-bit Mux can be replaced with Tri-State Buffers and a Decoder. [1 mark]

True False

(ii) Identify the size of the following values on the above diagram. [4 marks]

Value	No of Bits
k	
n	
p	
q	

Suppose the microprocessor supports the set of instructions in Table 1.

Table 1 – Instruction set.

Instruction	Description
ADD R_1, R_2	Add R_1 and R_2. $R_1 \leftarrow R_1 + R_2$
BTSC R	Test given bit, Skip if Clear
CLR R	Clear R. R ← 0
DEC R	Decrement R. R ← R – 1
GOTO *k*	Go to address *k*. PC ← *k*
INC R	Increment R. R ← R + 1
MOVL R, *l*	Move literal value *l* to R. R ← *l*
SUB R_1, R_2	Subtract R_1 and R_2. $R_1 \leftarrow R_1 - R_2$

As an example, ADD instruction can be further described as follows:

Instruction	ADD R_1, R_2			
Description	2's complement addition of register R_1 and R_2 and store results on R_1. $R_1 \leftarrow R_1 + R_2$, where $R_1, R_2 \in [0, 31]$			
***m*-bit instruction**	1 0 1	*k*-bits to indicate Register R_1	*k*-bits to indicate Register R_2	x

(iii) What is the word length *m* of an instruction? [2 marks]

a) 12 bits b) 13 bits
c) 14 bits d) 16 bits

(iv) According to Figure 1 what is the total capacity of the Program ROM in bytes? [2 marks]

a) 192 bytes b) 208 bytes
c) 224 byes d) 256 bytes

Considering the following Assembly code answer next 4 questions.

```
100: ADD 0x10, 0x5
101: BTSC Zero
```

(v) Write the machine code for the first instruction (i.e., `ADD`). [2 marks]

(vi) After executing the first instruction (i.e., `ADD`), what would be the values of Overflow and Zero flags? Assume values stored on registers $R_{0x10} = 56$ and $R_{0x5} = 200$. [2 marks]

Overflow _____ Zero _____

(vii) Once the `ADD` instruction is decoded, what bit values will you set for each of the following as control inputs? [4 marks]

32-way 8-bit Mux connected to left input of Add/Sub Unit |___|___|___|___|___|

32-way 8-bit Mux connected to right input of Add/Sub Unit |___|___|___|___|___|

Register Enable |___|___|___|___|___|

Add/Sub Select |___|

(viii) When `BTSC` instruction is decoded, what bit values will you set for each of the following as control inputs? Assume values stored on registers $R_{0x10} = 50$ and $R_{0x5} = 100$. [2 marks]

Jump Flag _____ Address to Jump _____

(ix) Write an Assembly program to multiply 2 numbers *x* and *y* using the instructions given in **Table 1**. You may use the general-purpose registers in Figure 1 to store initial, intermediate, and final values. Comment your code. [6 marks]

Question 2 **[25 marks]**

(i) Build a 4-to-1 multiplexer using 2-to-4 decoder. [4 marks]

(ii) Represent –2.72 using Single Precision, IEEE Floating Point standard. [4 marks]

Hint: Single Precision standard has a 23-bit mantissa, 8-bit exponent, and 1-bit sign. The exponent is calculated as $E = e + 127$.

(iii) "Above number can be represented more precisely using Double Precision, IEEE Floating Point standard." Do you agree or disagree with this statement? Explain. [2 marks]

(iv) Tick **TRUE** or **FALSE**. [1 × 10 marks]

		True	**False**
a)	Computer Architecture is the Blueprint/Plan that is visible to programmers.		
b)	A 64-bit RCA can be built using 64 half-adders.		
c)	A positive-edge (rising edge) triggered flip-flop changes the state when the clock signal changes from logic 0 to 1.		
d)	To change from $Q_t = 1$ to $Q_{t+1} = 0$, J and K inputs of a JK flip-flop need to be set as X, 1.		
e)	A good Instruction Set Architecture (ISA) provides convenient functions to higher layer (i.e., programmer) regardless of the complexity of hardware implementation at lower layer.		
f)	A flash ROM that can store 16K, 16-bit instructions has a memory capacity of 16KB.		
g)	Register Indirect Addressing allows large physical addresses to be accessed while having a few address bits in an instruction.		
h)	If sum of a positive number and a negative number yields a negative result, sum has overflowed.		
i)	Parallel buses give high throughput over short distances.		
j)	Polling is inefficient as it wastes CPU time.		

(v) Fill in the blanks using one of the following keywords: [1 × 5 marks]

`Buffered, CISC, Compulsory, Conflict, DMA, EEPROM, Interrupts, RISC, Slow, UVEPROM`

a) _____ processors support only a few basic set of instructions.

b) TV uses a _____ to remember the last channel viewed.

c) A cache placement strategy that is not fully associative causes _____ misses.

d) _____ provides a way to bypass the CPU when transferring data between memory and IO.

e) _____ data transfer is used when CPU is reading/writing from/to slow IO devices.

Question 3 **[25 marks]**

(i) "*Mobile processors are unlikely to have a Level 3 cache in near future*." Do you agree or disagree with this statement? Briefly Explain. [3 marks]

(ii) For a given application, 25% of the instructions require memory access. Instruction miss rate is 2% and data miss rate is 4%. L1 cache access time is 2 clock cycles while RAM access time is 50 clock cycles. Cache block size is 4 words.

1. How much time is required to access a word that is not in cache? [2 marks]

2. What is the average memory access time (for both instructions and data)? [3 marks]

(iii) Following program sum all the values in 2D array. Speed up the program by benefiting from spatial and/or temporal locality in caching. Justify your solution. [3 marks]

```
sum = 0
for (j= 0; j < n; j++)
    for (i = 0; i < m; i++)
        sum += a[i][j]
```

(iv) Suppose $m = 100$ and $n = 200$ in above program (i.e., Q3(iii)). How many clock cycles will be lost due to branching, if the branch penalty is 1 clock cycle? [3 marks]

(v) Modify your optimized program in Q3(iii) to reduce the loss of clock cycles due to branching. Explain why it will reduce lost clock cycles. [3 marks]

(vi) Given an integer x, write an Assembly program to generate $2x$, $3x$, and $4x$. For example, if $x = 4$, 3 designated registers should contain 8, 12, and 16.

Assume the microprocessor has 20, 8-bit general purpose registers labelled as R1, R2, … R20. $x \in [0, 63]$. It is ok to assume x is already stored in a general-purpose register. Use only the instruction set given as **Annex**. Comment your code. [8 marks]

Question 4 **[25 marks]**

(i) Using the production line that you observed during the field visit as an example, briefly explain how pipelining improves throughput but not latency. [4 marks]

Answer the questions in the context of following article.

The ARM Cortex-A75 processor is ARM's latest and highest-performance CPU delivering ground-breaking performance and market-leading power efficiency. The processor is broadly applicable from cloud to edge applications, providing improvements in performance, efficiency, and architecture over its predecessors. With significantly improved integer performance, and substantial enhancements in floating point and memory performance, the Cortex-A75 processor is the most powerful Cortex-A processor to date.

Cortex-A75 has 4 cores that support A64 ISA. A75 provides a significant boost in single-thread performance using a fully out-of-order, variable-length, and symmetrical three-way superscalar pipeline. A75 has a shared L3 cache (up to 4MB), support variable frequencies, and potentially independent voltage and power gating for individual or groups of Cores. A75 also uses a private 512KB L2 cache per core with half the latency of traditional high-performance processors. Both the I and D caches are 64KB each. A75 supports large memories with 44-bit physical memory addresses. It provides 20% more integer core performance compared to previous A72 and A73 processors.

– Parts of the write up are extracted from https://developer.arm.com

(ii) Tick **TRUE** or **FALSE**. [1 × 4 marks]

		True	**False**
a)	One way to improve memory performance is to increase the width of the data bus.		
b)	One way to improve integer and floating-point performance is to build multiplication and division units in hardware.		
c)	Each A64 instruction requires the same number of clock cycles.		
d)	Cortex-A75 executes instructions exactly in the same order as they are given in a program.		

(iii) Out of the following techniques in Cortex-A75, which ones reduce the power consumption? [2 marks]

1. Use of variable frequencies
2. Independent voltage control
3. Independent power gating

a) 1 and 2 only
b) 2 and 3 only
c) 1 and 3 only
d) 1, 2, and 3

(iv) With the suggested changes, overall speed up of integer performance is 20%. If integer unit is used 60% of the total time, what is the speed up of the overall system? [2 marks]

Hint: You may use the Amdahl's law to calculate the speed up.

$$Speedup_{Overall} = \frac{1}{(1 - Fraction_{Enhanced}) + \frac{Fraction_{Enhanced}}{Speedup_{Enhanced}}}$$

a) 0.9
b) 1.11
c) 1.2
d) 2.0

(v) What is the maximum size of RAM supported by Cortex-A75? [2 marks]

(vi) Draw the cache hierarchy of Cortex-A75. Clearly label the diagram. [5 marks]

(vii) "*While ARM has not announced about the max clock speed of Cortex-A75, we believed that it further increased from the previous generation Cortex-A73, which supported a max frequency of 2.8 GHz*".

Do you agree or disagree with this statement? Briefly discuss. [3 marks]

(viii) As Cortex-A75 has significant power, energy, and cost performance compared to other commercial processors, Smart Computing Sri Lanka (Pvt) Ltd. plans to build low-end servers targeting office-automation applications. What challenges need to be overcome to build such low-end servers in Sri Lanka? [3 marks]

---------- END OF THE PAPER ----------