Index No:							

UNIVERSITY OF MORATUWA

Faculty of Engineering

Department of Computer Science & Engineering

B.Sc. Engineering
2017 Intake Semester 2 Examination

CS2052 COMPUTER ARCHITECTURE

Time allowed: 2 Hours 10 min December 2018

ADDITIONAL MATERIAL: *None*

INSTRUCTIONS TO CANDIDATES:

1. **10 minutes** of reading time is provided in addition to **2 hours** allocated.
2. This paper contains **4** questions on **13** pages.
3. This examination accounts for 60% of the module assessment.
4. This is a closed book examination.
5. Answer **ALL** questions.
6. Answer the questions on the paper itself and within the given space.
7. Applicable Assembly instructions are given as **Annex**.
8. For MCQ and True/False questions, select the most appropriate answer. No penalty for wrong answers.
9. The maximum attainable mark for each question is given in brackets.
10. Only calculators approved by the Faculty of Engineering are permitted.
11. Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions made on the script.
12. If you have any doubt as to the interpretation of the wording of a question, make your own decision, but clearly state it on the script.
13. Electronic/Communication devices are not permitted. Only equipment allowed is a calculator approved and labelled by the Faculty of Engineering.
14. This paper should be answered only in English.

Q1	Q2	Q3	Q4	Total

Question 1 **[25 marks]**

ATtiny13 is a high-performance, low-power microcontroller by Atmel. Figure 1 shows the block diagram of ATtiny13. ATtiny13 supports 120, 16-bit RISC instructions. Each data word is 8-bits and can be stored in one of the following physical memory elements:

- 1K Bytes of Self-programmable Flash memory
- 64 Bytes EEPROM
- 64 Bytes Data SRAM

Data SRAM can also be used as Stack. I/O Lines is a 6-bit bi-directional I/O port. Operating voltage of ATtiny13 can be varied from 2.7 - 5.5V while also varying the clock rate between 10 and 20 MHz. Minimum power consumption during active mode is 240 µA while sleep mode consumes 0.1 µA.

Answer following questions based on Figure 1 and above description.

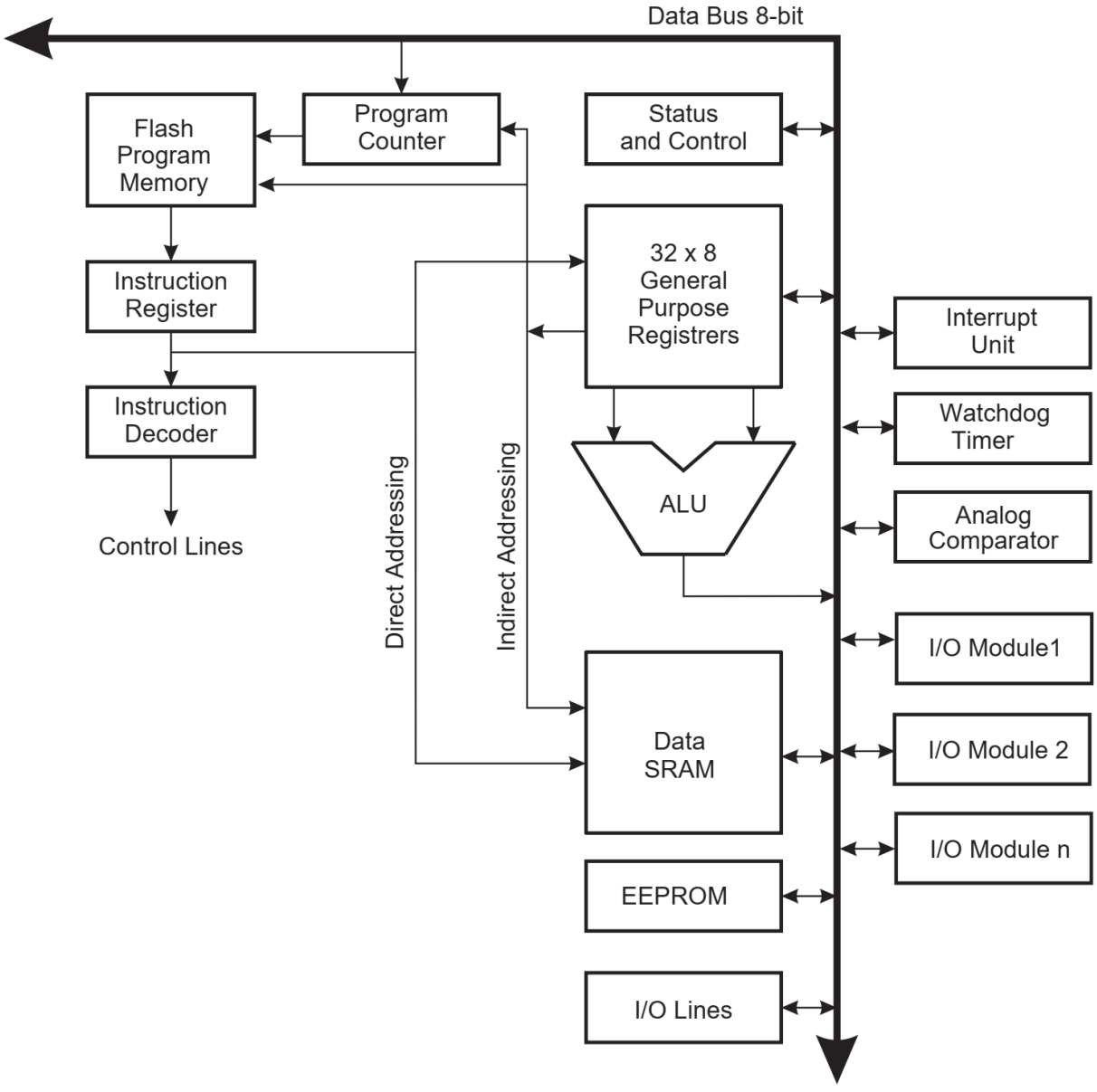


Figure 1 – High-level architecture of ATtiny13.

(i) Tick **TRUE** or **FALSE**. [1 × 10 marks]

		True	False
a)	ATtiny13 design is based on the Harvard Architecture.		
b)	While there is no Accumulator in Figure 1, same behavior could be obtained using one of the General Purpose Registers.		
c)	Data stored in the EEPROM is lost when power is switched off.		
d)	Stack is 16-level deep.		
e)	ATtiny13 enables Register Indirect Addressing, by storing an Address in the Data SRAM and then loading the value into the Program Counter.		
f)	Compared to polling, interrupt unit helps to improve the efficiency of the microcontroller.		
g)	Due to the use of I/O Modules, input/output devices connected to ATtiny13 must use the same clock speed.		
h)	ADDLW type instructions cannot be supported as the Instruction register is not directly connected to the ALU.		
i)	Minimum energy consumption during active mode is achieved when the microcontroller is powered up at 5.5 V.		
j)	ATtiny13 will consume more power while running at 20 MHz compared to running at 10 MHz		

(ii) How many bits are quired to uniquely address each of the following memory? [4 marks]

a) General Purpose Registers _____ c) EEPROM _____

b) Self-programmable Flash Memory _____ d) Data SRAM _____

Table 1 lists a subset of instructions supported by ATtiny13.

Table 1 – Instruction set.

Instruction	Description
ADD R_1, R_2	Add R_1 and R_2. $R_1 \leftarrow R_1 + R_2$
SBRC R, b	Test bit *b* on register R, Skip if Clear
CLR R	Clear R. R ← 0
DEC R	Decrement R. R ← R – 1
LDI R, *k*	Load immediate value *k* to R. R ← *k*
MOV R_1, R_2	Move between registers. $R_1 \leftarrow R_2$
SUB R_1, R_2	Subtract R_1 and R_2. $R_1 \leftarrow R_1 - R_2$

Considering the following Assembly code answer the next set of questions.

```
100: LDI 0x10, 0xF0
101: LDI 0x5, 0x0F
102: ADD 0x10, 0x5
103: SBRC 0x10, 0
104: DEC 0x10
```

(iii) After executing the 3rd instruction (i.e., `ADD`), what would be the values of Overflow and Zero flags? [2 marks]

Overflow _____ Zero _____

(iv) Will the instruction at address 104 get executed? Briefly explain why. [2 marks]

(v) Write an Assembly program to swap the values in 2 registers R_{10} and R_{20} using the instruction set given in **Table 1**. You may use the general-purpose registers to store initial, intermediate, and final values. Comment your code. [5 marks]

(vi) Given a data address (e.g., in Direct Addressing), how can we differentiate whether it should go to General Purpose Registers or Data SRAM? [2 marks]

Question 2 **[25 marks]**

(i) Fill in the blanks using one of the following keywords: [1 × 8 marks]

```
Associativity | CISC | Code | Direct | HDDs | Indexed |
Instruction Register | Isolated | Memory Mapped | Parallel |
Program Counter | Prefetching | RISC | Serial | SSDs | Stack
```

a) When a program is loaded into the memory _____ segment contains the set of instructions.

b) MOV R5, Table[3] is an example of _____ addressing.

c) For data transfer inside the CPU _____ busses are preferable as they provide high throughput data transfer.

d) _____ enables proactive loading of instructions and data assuming they may be useful in the future.

e) While _____ enable high throughput, low latency, and persistent data storage, they are relatively expensive.

f) _____ instructions are easier to pipeline, as they enable basic operations that can be represented in a few formats while supporting fewer addressing modes.

g) In _____ I/O, devices and memory share the same address space.

h) Before processing an interrupt, CPU first stores the current _____ value and register values (i.e., process state).

Boltzmann constant is $1.38064852 \times 10^{-23}$ m^2 kg s^{-2} K^{-1}

(ii) *"It is sufficient to represent the Boltzmann constant using Single Prevision."*

Do you agree or disagree with this statement? Discuss. [3 marks]

Hint: Single Precision IEEE standard has a 23-bit mantissa, 8-bit exponent, and 1-bit sign. The exponent is calculated as $E = e + 127$. Whereas Double Precision standard uses 52-bit mantissa and 11-bit exponent. The exponent is calculated as $E = e + 1023$.

(iii) Represent only the mantissa of the Boltzmann constant (i.e., 1.38064852) using Single Precision IEEE Standard. [4 marks]

(iv) Derive a logic circuit using D Flip Flops to count from 0 to 9. Once the counter reaches 9, it returns back to 0. Such a counter is referred to as the Binary Coded Decimal (BCD) counter. You answer should include truth table, k-Map, and logic circuit. [10 marks]

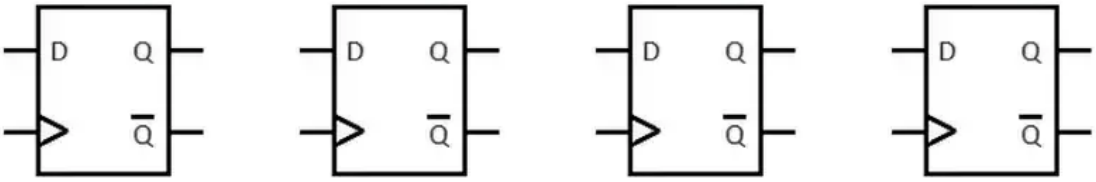
Q_t				Q_{t+1}				D			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								

	00	01	11	10
00				
01				
11				
10				

	00	01	11	10
00				
01				
11				
10				

	00	01	11	10
00				
01				
11				
10				

	00	01	11	10
00				
01				
11				
10				



Question 3 **[25 marks]**

(i) Select the most appropriate answer. [2 ×3 marks]

a) What technical factor limits the growth of uni-processors?

a) Increasing power consumption.
b) Rising transistor count.
c) Inability to address larger memories.
d) Inability to execute instructions without using a pipeline.

b) Which of the following **does not** contribute to data access time of a hard disk?

a) Platter latency
b) Read time
c) Rotational delay
d) Seek time

c) Which of the following statements is true about multi-core processors?

a) Intel Hyper Threading (HT) in an example of a true multi-core processor.

b) L1 cache is always shared among multiple cores.

c) Multi-cores do not follow Moore's Law.

d) Multiple cores increase the throughput of a processor.

(ii) For a given application, 20% of the instructions require memory access. Instruction miss rate is 2% and data miss rate is 4%. L1 cache access time is 4 clock cycles while RAM access time is 50 clock cycles. Cache block size is 4 words.

a) How much time is required to access a word that is not in cache? [2 marks]

b) What is the average memory access time (both instructions and data)? [3 marks]

(iii) Given 2 integers n and x ($1 \leq n \leq 5$, $1 \leq x \leq 20$), suppose we want to calculate nx. Before the calculation we first need to store n and x on 2 General Purpose Registers (GPRs).

a) Write an Assembly program to calculate nx. Assume that the microprocessor has 20, 8-bit GPRs labelled as R1, R2, …, R20. Use only the instruction set given as **Annex**. Comment your code. [8 marks]

b) Suppose a more advanced version of the PIC microcontroller provides the following multiplication instructions:

```
MULWF f, d ; (W)×(f) → (W) or (f). If d = 0 results in W else f
MULLW k    ; (W)×k → (W)
```

What changes are required in your solution for Question III(a) to calculate x^n? Assume n and x values will be chosen such that x^n will always be ≤ 255. [3 marks]

c) "*If we use the program in Question III(b), it will take more time to calculate* 6^3 *compared to* 2^3."

Do you agree or disagree with this statement? Briefly discuss. [3 marks]

Question 4 **[25 marks]**

(i) Modern memory hierarchy integrates many layers of memories to bridge the Processor-Memory Gap. Using Solid State Disk (SSD), Intel Optane Non-volatile Memory, or Flash Memory in Pen Drives as an example, explain how the latency gap between the RAM and Hard Disk could be reduced. [5 marks]

Answer the questions in the context of following article.

NXP® Semiconductors's MPC7447 processor achieves two major milestones in the embedded world: It delivers 1.3 GHz of performance. It also dissipates less than 10W while running at 1GHz. This innovative processor built on PowerPC Architecture provides best-in-class solution for networking, telecommunication, and computing product OEMs. Processors based on Power Architecture enjoy the broadest set of operating systems, compilers, and development tools from third-party tool vendors belonging to NXP Connect partner program.

MPC7447 is a high-performance, low-power 32-bit implementation of the RISC architecture. It features a high-frequency superscalar core capable of issuing 4 instructions per clock cycle (3 instructions + branch) into eleven independent execution units. Its 7-stage pipeline enables 1.0 instruction per clock cycle throughput for most instructions.

The MPC7447 can reach speeds of 1.3 GHz with a core voltage of 1.3V and includes 512KB of on-chip L2 cache. Separate on-chip L1 instruction and data caches follow the Harvard architecture. Both I and D cache are 32-Kbyte, 8-way set associative. L1 and L2 cache block sizes are 32-byte and 64-byte, respectively. Parity checking support is provided on L1 and L2 cache arrays. 36-bit physical address space can directly address memory while feeding data via a high-bandwidth 133 MHz 64-bit MPX Bus/60x Bus.

A lower-power version of the MPC7447 is also available, operating at speeds of up to 1 GHz with a core voltage of 1.0V. It further supports 3 power-saving user-programmable modes to reduce power drawn by processor.

– Parts of the write up are extracted from nxp.com

(ii) Tick **TRUE** or **FALSE**. [1 × 9 marks]

		True	False
a)	Embedded processors typically tradeoff cost and energy over speed.		
b)	MPC7447 enables executing at most 4 instructions simultaneously without duplicating all processor components.		
c)	MPC7447 is a multi-core processor.		
d)	Parity can detect 1-bit instruction or data errors while in cache memory.		
e)	GOTO is a conditional branch instruction.		
f)	All PowerPC instructions on MPC7447 pipeline should have the same number of stages.		
g)	As MPC7447 pipeline has 7-stages, branch penalty is 1 clock cycle.		
h)	A cache block can be moved to one of the 8 locations.		
i)	Bandwidth of Memory bus depends only on clock speed (e.g., 133 MHz)		

(iii) Out of the following techniques in MPC7447, which ones reduce the power consumption? [2 marks]

1. Use of variable frequencies
2. Use of variable voltage
3. Independent power gating

a) 1 and 2 only
b) 1 and 3 only
c) 2 and 3 only
d) 1, 2, and 3

(iv) MPC7447 has 2× increase in cache memory compared to previous version MPC7445. With this improvement, overall memory access latency is improved by 15%. If memory unit is used 30% of the total time, what is the speed up of the overall system? [2 marks]

Hint: You may use the Amdahl's law to calculate the speed up.

$$Speedup_{Overall} = \frac{1}{(1 - Fraction_{Enhanced}) + \frac{Fraction_{Enhanced}}{Speedup_{Enhanced}}}$$

a) 0.3
b) 1.04
c) 0.7
d) 1.10

(v) What is the maximum size of RAM supported by MPC7447? [2 marks]

(vi) Draw the cache hierarchy of MPC7447. Clearly label the diagram. [5 marks]

(vii) As MPC7447 has significant power, energy, and cost performance compared to other embedded processors, Link Lanka (Pvt) Ltd. plans to build networking devices (e.g., wireless access points and routers) targeting home users. What challenges need to be overcome to build such networking devices in Sri Lanka? [5 marks]

---------- END OF THE PAPER ----------