UNIVERSITY OF MORATUWA

FACULTY OF ENGINEERING

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

B.Sc. Engineering
2012 Intake Semester 2 Examination

CS2052 COMPUTER ARCHITECTURE

Time allowed: 2 Hours June 2014

ADDITIONAL MATERIAL: *None*

INSTRUCTIONS TO CANDIDATES:

1. This paper consists of **5** questions in **5** pages.
2. Answer ALL questions.
3. Start answering each of the main questions on a new page.
4. The maximum attainable mark for each question is given in brackets.
5. This examination accounts for 60% of the module assessment.
6. This is a closed book examination.

   NB: It is an offence to be in possession of unauthorised material during the examination.
7. Only calculators approved by the Faculty of Engineering are permitted.
8. Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions made on the script.
9. In case of any doubt as to the interpretation of the wording of a question, make suitable assumptions and clearly state them on the script.
10. This paper should be answered only in English.

Question 1 **[20 marks]**

Figure 1 shows the block diagram of a simple microprocessor (a.k.a. nanoprocessor). Answer following questions based on Figure 1.

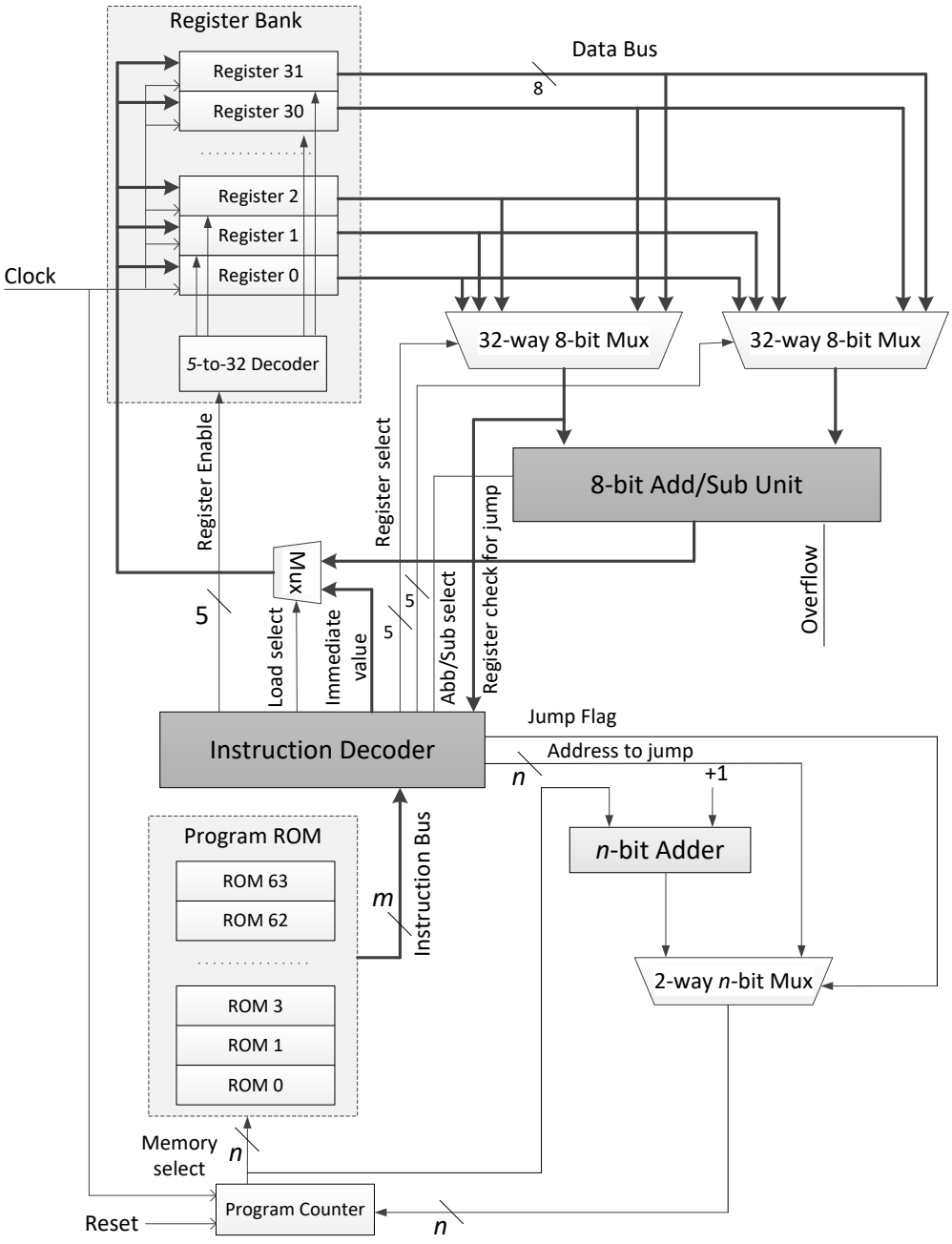

Figure 1 – High-level diagram of the microprocessor.

(i) "This microprocessor is based on the Harvard Architecture". Do you agree or disagree with this statement? Provide one sentence justification. [2 marks]

(ii) Using the 2's Complement calculate 34 – 125. Note that registers are 8-bit. [3 marks]

(iii) Calculate the size of Program Counter (i.e., number of bits *n* in Figure 1). [2 marks]

Assume Registers 0 and 1 are hardcoded with values 0 and 1, respectively. Then one of the instructions supported by the microprocessor can be defined as follows:

Instruction	INC R			
Description	Increment register R, i.e., $R \leftarrow R + 1$. $R \in [0, 31]$			
***m*-bit instruction**	1 0 1	*n*-bits to indicate Register R	*n*-bits to indicate Register 1	x x x x

(iv) What is the word length of an instruction? [2 marks]

(v) Write the machine code for the following instruction. [3 marks]

```
INC 0x15
```

(vi) Briefly explain how the above instruction can be implemented on the microprocessor. Clearly identify what components to activate and how to activate them. [6 marks]

(vii) If the Program ROM can store 64 such instructions, what is the total capacity of the Program ROM in bytes? [2 marks]

Question 2 **[20 marks]**

(i) Represent 3.4375 using Single Precision, IEEE Floating Point standard. [5 marks]

Hint: Single Precision standard has a 23-bit mantissa, 8-bit exponent, and 1-bit sign. Exponent is calculated as $E = e + 127$.

(ii) Show the schematic diagram of a 4-to-1 multiplexer built using a decoder and other basic logic components. [3 marks]

(iii) A 3-bit counter has the following sate transitions:

000 → 001 → 011 → 111 → 000 → 001 → 011 → 111 → 000 → …

Show the schematic diagram of this counter built using T Flip Flops. Your answer should include the truth table, Karnaugh Maps, and schematic diagram. [12 marks]

Question 3 **[20 marks]**

(i) Briefly describe 2 advantages of programming in Assembly language vs. high-level languages. [4 marks]

(ii) Given an integer x, write an Assembly program to calculate its power x^2. For example, if $x = 3$, $x^2 = 9$. Comment your code. [12 marks]

Assume the microprocessor has 20, 8-bit general purpose registers labelled as R1, R2, … R20. $x \in [1, 15]$. Use only the instruction set given in Appendix (see page 5).

(iii) Describe Direct/Register addressing, using one of the Assembly instructions in your program (Question 3(ii)) as an example. [2 marks]

(iv) "Sleep instruction puts the microprocessor to standby mode". Describe the meaning of this statement. [2 marks]

Question 4 **[20 marks]**

Part of the following write up is extracted from "Evaluating Intel's Many Integrated Core Architecture for Climate Science" by Theron Voran, Jose Garcia, and Henry Tufo.

> Knights Ferry (KNF) is the 1st generation of Intel's Xeon Phi Architecture. KNF is implemented on a PCIe (express) card plugged into a desktop/server system. The KNF card has up to 32 cores (each clocked up to 1.2 GHz) supporting 4 hardware threads per core and a short pipeline.
>
> Each core is provided an 8-ways set associative 32KB L1 data cache and a 32KB L1 instruction cache, as well as a 256KB L2 cache. The L2 caches for each core are interconnected via a bidirectional ring bus, creating an 8MB globally-shared cache. Additionally the KNF cores share 1 or 2GB of DDR5 main memory. L1 cache access time is approximately 3 clock cycles. L1 miss penalty is 72 clock cycles.

Based on the above description answer the following questions.

(i) Calculate the total number of hardware-level threads in KNF. [3 marks]

(ii) Briefly explain what is meant by a "short pipeline" [4 marks]

(iii) Briefly explain what is meant by a "8-ways set associative" [3 marks]

(iv) For a given application, 50% of the instructions require memory access. Miss rate is 2%. An instruction can be executed in 1 clock cycle. Calculate the average memory access time. [5 marks]

(v) Draw the cache/memory hierarchy of KNF while labelling necessary components and their capacities. No need to draw all the cores. [5 marks]

Question 5 **[20 marks]**

Suppose you join Smart Computing Solutions Inc. as in intern. Your team is responsible for designing a new energy-efficient server using microprocessors that are typically used in smart phones (a.k.a. mobile processors). As a preparation for the first project meeting, each team member is asked to think about how to implement various components of the server. Even though you are an intern, you are also asked to contribute as you have taken a class in Computer Architecture.

(i) What are the advantages and disadvantages of using a mobile processor vs. a desktop or server class processor? [4 marks]

(ii) For each of the following pair of options, what would you recommend for the proposed server? Justify your recommendation.

a. A CISC or a RISC processor [4 marks]

b. A 32-bit or a 64-bit processor [3 marks]

c. A Hard Disk or a Solid State Disk [3 marks]

(iii) What particular challenges need to be overcome, if Smart Computing Solutions Inc. wants to build and assemble the server in Sri Lanka? Briefly explain 3 challenges with examples. [6 marks]

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